REMARKS

The Office Action dated February 28, 2005, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claim 1 has been amended. Applicant submits that the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Claims 1-8 are pending in the present application and claims 1, 2 and 5 are respectfully submitted for consideration.

Allowable Subject Matter

As a preliminary matter, Applicant appreciates the allowance of claims 3, 4 and 6-8.

Claims 1, 2 and 5 Rejected under 35 U.S.C. § 102(b)

Claim 1, 2 and 5 were rejected under 35 U.S.C. §102(b) as being anticipated by Applicant Admitted Prior Art ("AAPA"). Applicant respectfully traverses the rejection and submits that each of these claims recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 1 recites a delay time adjusting method comprising, among other features, the step of increasing the delay time when a phase difference detected in the step of comparing indicates that said output signal is ahead of or behind the input signal.

Claim 5 recites a delay time adjusting circuit comprising, among other features, a delaying circuit for increasing a delay time of said phase of said output signal, when starting the delay time adjustment, so that the delay time is set to a value at which said phase difference becomes N periods, where N is an integer other than zero.

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It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicants' invention.

The Office Action characterized Figures 1 and 3 of AAPA as allegedly disclosing "a delay time adjusting circuit with a corresponding method of adjusting a delay time of an input signal [Cin] so that a phase of the input signal and a phase of an output signal [Cout] match each other ... and ... starting an increase of the delay time whenever a phase difference is detected in the step of comparing ... and [having] a delay circuit for increasing a delay time of the phase of the output signal when starting the delay time adjustment so that the delay time is set to a value at which the phase difference becomes N periods, where N is an integer other than zero."

Applicant respectfully disagrees with the characterization of Figures 1 and 3 of AAPA, and submits that AAPA fails to disclose or suggest each and every element recited in claims 1 and 5 of the present application. In particular, it is submitted that the delay time adjusting method and circuit of AAPA are neither comparable nor analogous to the delay time adjusting method and circuit of the claimed invention.

For example, AAPA fails to disclose the feature of increasing the delay time when a phase difference is detected such that the output signal is ahead of or behind the input signal. Furthermore, AAPA does not show that the delay time is set to a value at which the phase difference becomes N periods.

In AAPA, the signal dclk (Fig. 3(e)) is obtained by delaying the signal Cin by the DLL ARRAY 3 and divided by the FREQUENCY DIVIDER 4 and further delayed by the DUMMY CIRCUIT 6. The signal tclk of AAPA is obtained by dividing the signal Cin by the FREQUENCY DIVIDER 2. It is submitted that the FREQUENCY DIVIDER 4 divides

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the signal Cin but does not invert the phase while the FREQUENCY DIVIDER 2 inverts

the phase. Accordingly, tclk and dclk of AAPA have waveforms having inverted phase.

In essence, the first down-edge of tclk corresponds to the first up-edge. The DLL

ARRAY 3 is adjusted so as to generate the signal Lon when the first up-edge of tclk

matches the first up-edge of dclk. At this time, dclk is in synchronization with tclk with a

delay of one period, where one period is a time from a down-edge to a subsequent up-

edge of the signal tclk. That is, N is equal to 1 (N=1) and N cannot be equal to or

greater than 2. If N=0, this means that dclk is in synchronization with tclk without delay,

that is, the delay time of the DLL ARRAY 3 and the delay time of the DUMMY CIRCUIT

6 are zero, which cannot occur. Thus, N=0 never happens in AAPA.

In contrast, Figs. 6 and 7 of the present invention for example shows that N can

take a value equal to or greater than 2. For instance, Fig. 6 shows an example where

the frequency of the signal Cin, which is an external clock, is low; and Fig. 7 shows an

example where the frequency is high. In Fig. 6, the first up-edge of dclk is on the left

side of the first up-edge of tclk, and therefore, the first up-edge of dclk is synchronized

with the first up-edge of tclk by delaying dclk of the DLL ARRAY. However, the first up-

edge of dclk of Fig. 7 is on the right side of the first up-edge of tclk, and therefore the

first up-edge of dclk is synchronized with the second up-edge of tclk by delaying dclk of

the DLL ARRAY. In this case, N is equal to 3 (N=3).

It is submitted that if a high frequency is applied to AAPA, a malfunction occurs in

the DLL.

As discussed above, Applicant submits that N is fixed to only 1 (N=1) in the prior

art, while N is equal to 1 or 3 depending to the frequency of the signal Cin in the present

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invention. According to the present invention, N may be equal to 1 or 2 if a different circuit structure of the divider and the phase comparator is used.

It is an advantage of the present invention that a clock frequency of a large range can be used since the delay can be adjusted to one of a plurality of values of N such as N=1 or 3 in accordance with the clock frequency. In contrast, the delay is adjusted where N is always equal to 1 (N=1) in the prior art, which causes a problem when the clock frequency is high.

Therefore, Applicant submits that AAPA fails to disclose each and every element recited in claims 1 and 5 of the present application.

Moreover, to qualify as prior art under 35 U.S.C. §102, a single prior art reference must teach, i.e., identically describe, each feature of a rejected claim. As explained above, AAPA fails to disclose or suggest each and every feature of claims 1 and 5. Accordingly, Applicant respectfully submits that claims 1 and 5 are not anticipated by AAPA. Therefore, Applicant respectfully submits that claims 1 and 5 are allowable.

As claim 2 depends from claim 1, Applicant submits that claim 2 incorporates the patentable aspects therein, and is therefore allowable for at least the reasons set forth above with respect to the independent claim, as well as for the additional subject matter recited therein.

Accordingly, Applicant respectfully requests withdrawal of the rejection.

Conclusion

In view of the above, Applicant respectfully submits that each of claims 1, 2 and 5 recites subject matter that is neither disclosed nor suggested in the cited prior art.

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Applicant also submits that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 1, 2 and 5 be found allowable and that this application be passed to issue along with allowed claims 3, 4 and 6-8.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300.

Respectfully submitted,

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